Exhibit 12

[redacted]

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC., MICRON SEMICONDUCTOR PRODUCTS, INC., and MICRON TECHNOLOGY TEXAS LLC

Petitioners,

v.

NETLIST, INC.,

Patent Owner.

Patent No. 11,016,918

Inventors: Chi-She Chen, Jeffrey C. Solomon, Scott H. Milton, and Jayesh Bhakta

TITLE: Flash-DRAM Hybrid Memory Module

Inter Partes Review No. IPR2023-00406

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 11,016,918

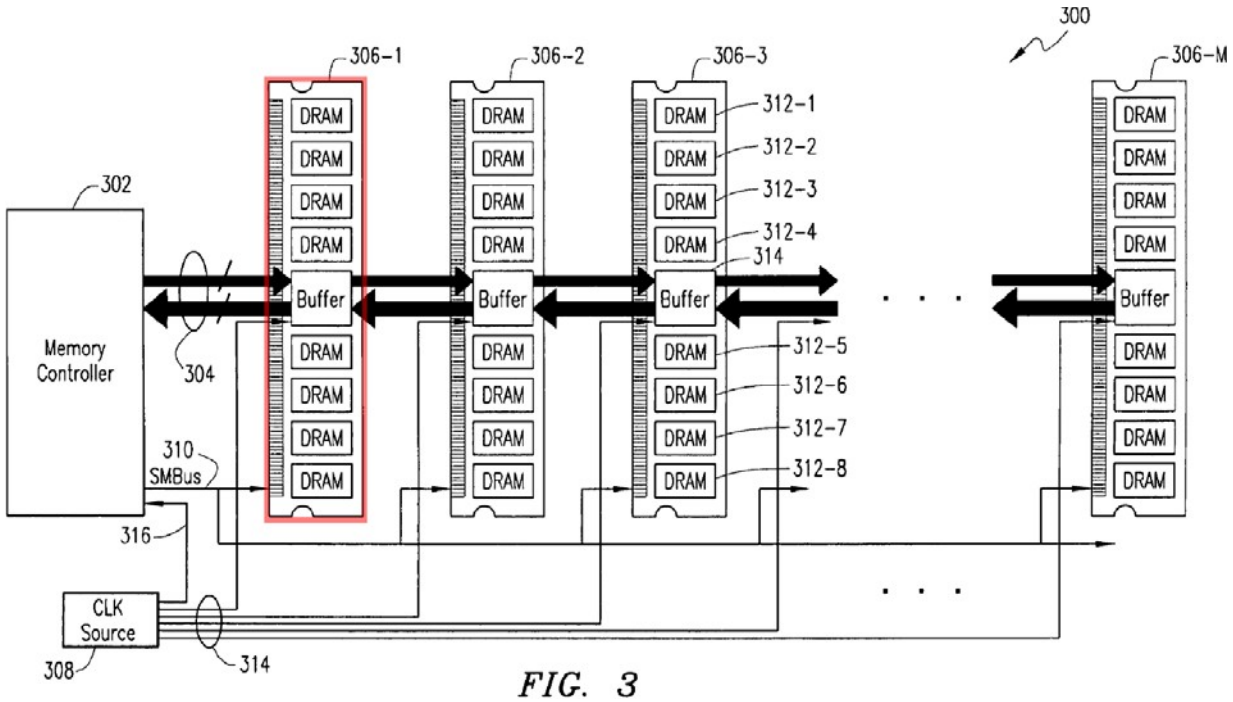
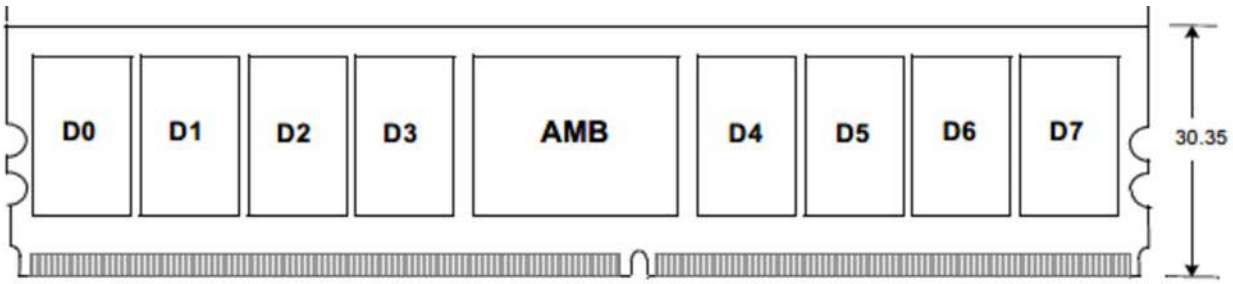


FIG. 3

A POSITA would have recognized the FBDIMM "*memory module[s]*" disclosed by Harris (above) are similar to the "*memory module[s]*" disclosed in JEDEC's FBDIMM Standards (e.g., below):



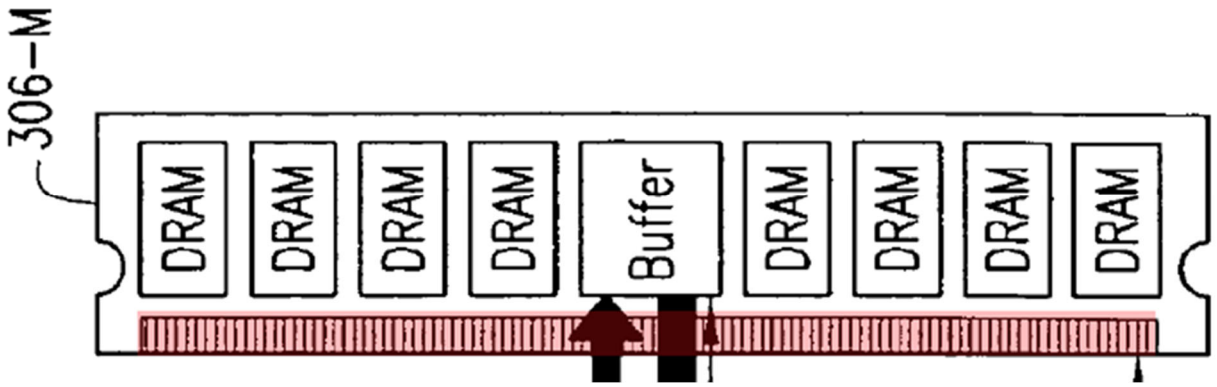
EX1028, p.38; EX1003, ¶221.

b) [1.b]

Grounds 1A-1C teach "*a printed circuit board (PCB)*," as shown above for [1.a]. *See also* EX1023, ¶[0013] ("printed circuit board"), ¶[0009] ("memory board"), Figs.1A, 3; EX1028, pp.10 ("PCBs are called … 'raw cards'"), 38, 84;

EX1003, ¶¶223-225.

Grounds 1A-1C teach the PCB "having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections" (sometimes called "pins") as shown above for [1.a] and reprinted below from Harris's Figure 3. EX1023, ¶¶[0002, 12-13, 19], Figs. 3-4; EX1028, pp.38, 84; EX1003, ¶¶226-227.



Grounds 1A-1C teach the edge connections in Harris, consistent with JEDEC's FBDIMM Standards, are "*configured to couple power, data, address and control signals between the memory module and the host system*":

- "*power*": EX1023, ¶[0012] ("power"/"+12V" "pins"); *id.*, ¶¶[0010, 19] & Fig.1A (104, below).

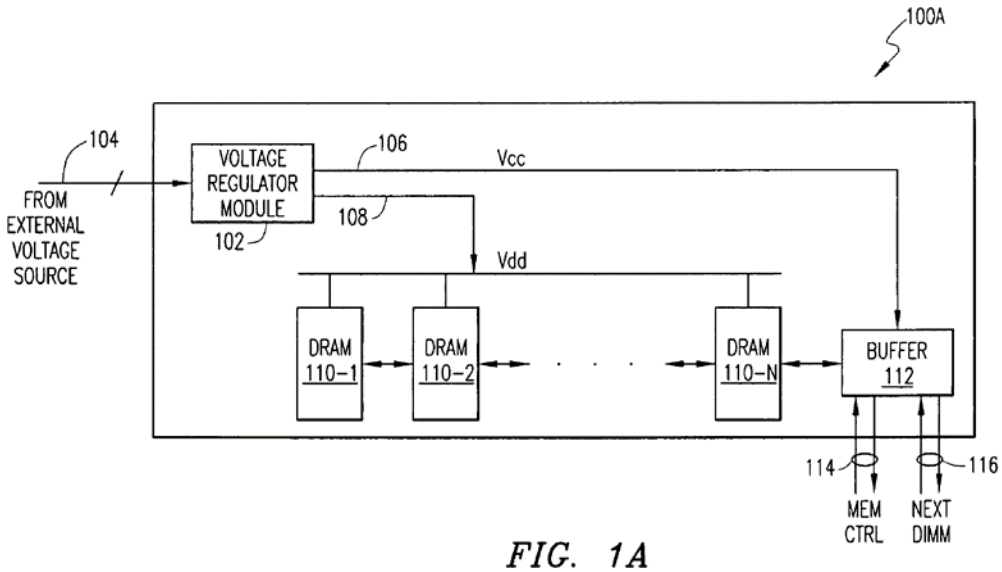


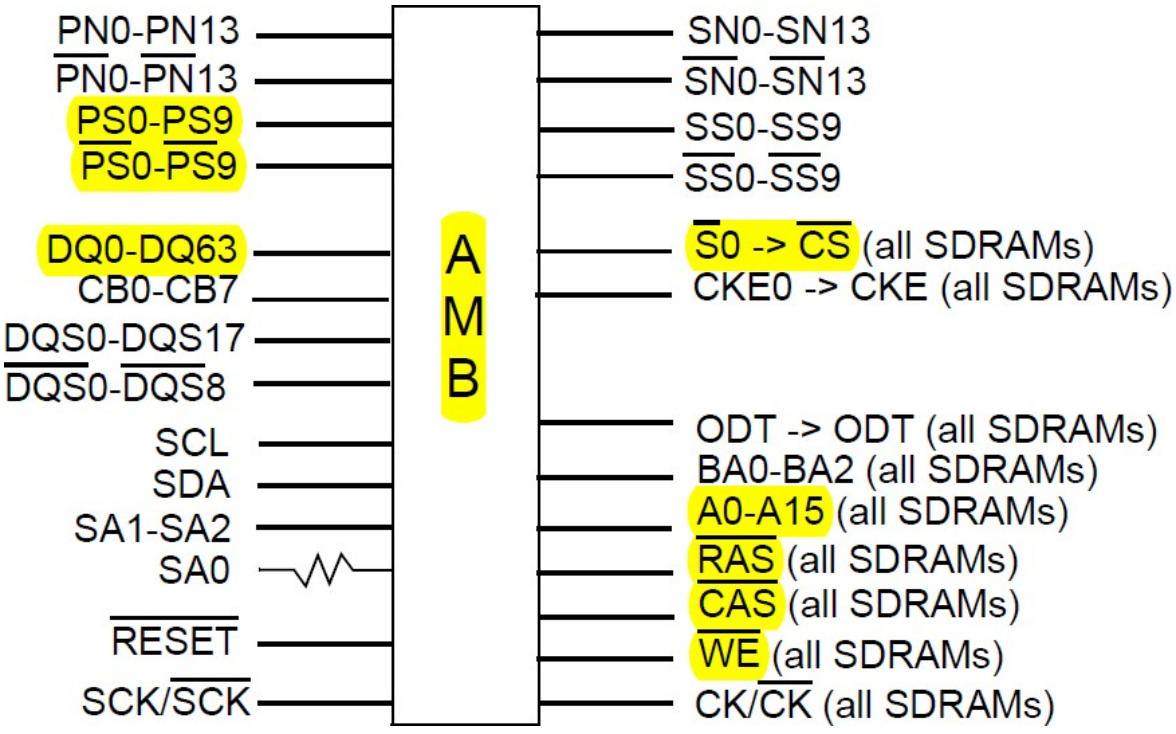
FIG. 1A

Furthermore, as shown in Figure 1A above, Buffer 112 (called "AMB" in the FBDIMM Standards) receives via 114 and transmits to DRAMs 110-1 to 110-N the following signals (as shown below and consistent with JEDEC standards):

- "*data*": e.g., DQ0-DQ63 (below); EX1023, ¶[0009] ("buffer/logic component 112 is provided for buffering command/***address*** (C/A) space as well as ***data*** space at least for a portion of the memory devices 110-1 through 110-N")
- "*address*": e.g., A0-A15 (below); *id.* ("***address***")
- "*control*": e.g., RAS, CAS, WE, CS (below); *id.* & Fig.1A (114, "CTRL"). These "*control*" signals together can form a "command." *See, e.g.*, EX1028, p.29 ("Part of command"); EX1026, pp. 6 ("RAS, CAS and WE (along with CS) define the command"), 46-47, 52.

See also EX1023, ¶¶[0009-12, 17, 19], Figs.1A, 3; EX1028, pp.11, 13 (below), 29;

EX1027, pp.1 (AMB "[a]cts as DRAM memory buffer for all read, write, and configuration accesses addressed to the DIMM"), 3-4 (below, "The southbound input link is 10 lanes wide and carries commands and write data from the host….The northbound input link is 13 to 14 lanes wide and carries read return data…back towards the host… There are two copies of address and command signals [output from the AMB to the SDRAMs] to support DIMM routing and electrical requirements."), 7 ("Southbound: The direction of signals running from the host controller toward the DIMMs."), 81-82; EX1026, pp. 6, 46-47, 52; EX1003, ¶¶228-231.



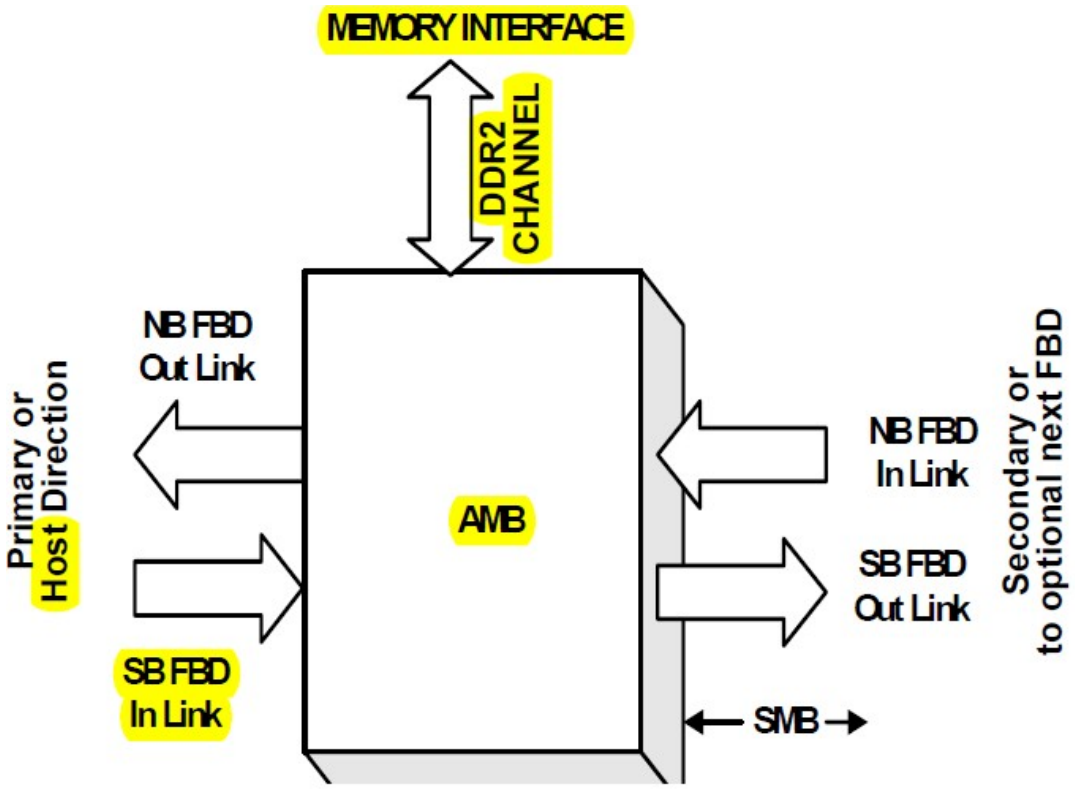


Figure 1.2 — Advanced Memory Buffer Interfaces

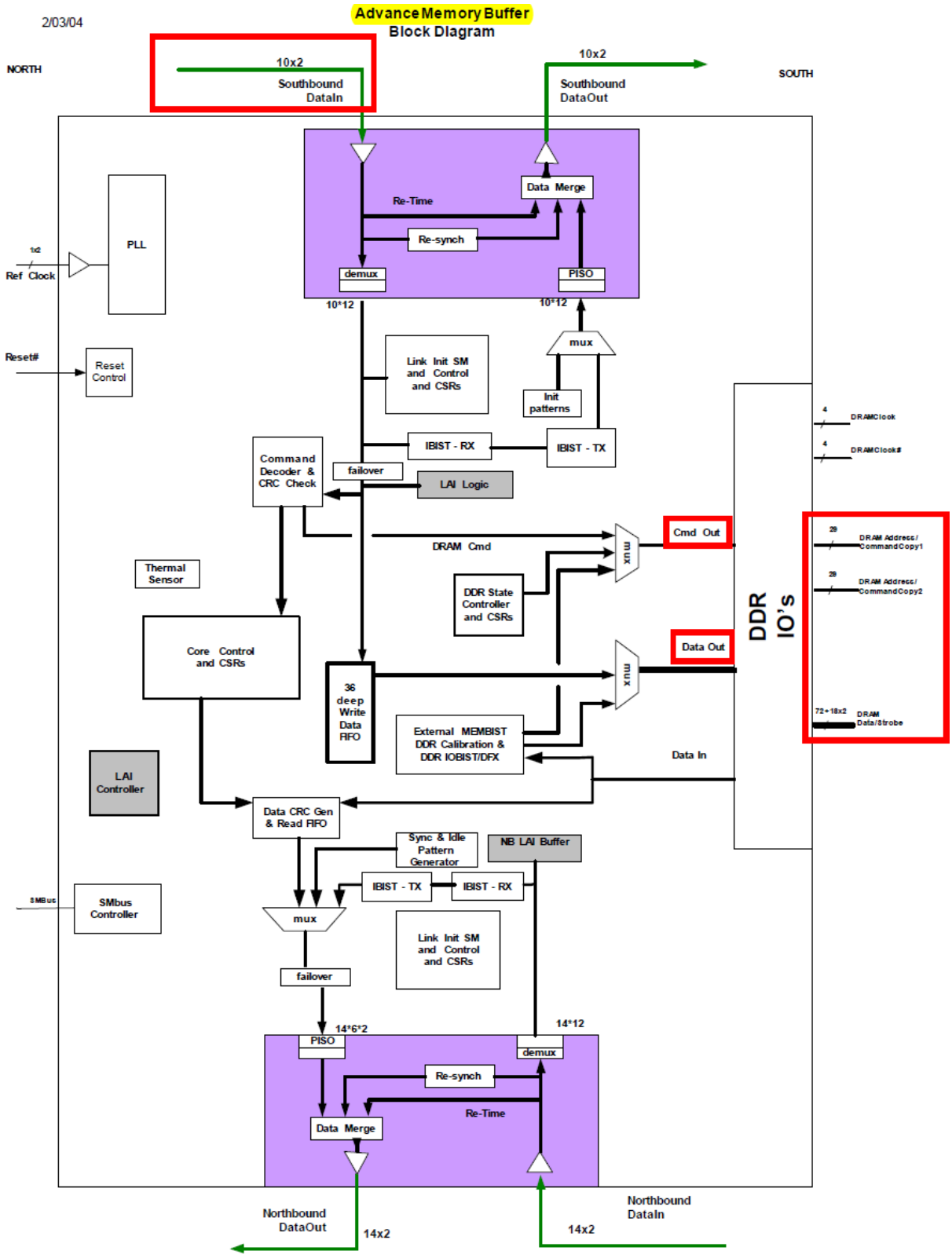


Figure 1.1 — Advanced Memory Buffer Block Diagram